In re Patent Application of
ERRATICO
Serial No. **09/899,573**
Filed: **JULY 5, 2001**

REMARKS

Applicant thanks the Examiner for the careful and thorough examination of the present application. By this amendment, Independent Claims 12, 17, and 22 have been amended to more clearly define the subject matter thereof over the prior art. Support for the amendments may be found on pages 8, 9 and 15 of the specification, for example. No new matter is being added. Claims 12-26 remain pending in the application. Favorable reconsideration is respectfully requested.

I. The Claimed Invention

The present invention is directed to a Bipolar-CMOS-DMOS (BCD) integrated circuit. As recited in amended independent Claim 17, for example, the integrated circuit includes a substrate having a first conductivity type and an epitaxial layer on the substrate. The epitaxial layer has the first conductivity type and a conductivity less than a conductivity of the substrate. Moreover, the integrated circuit also includes first and second regions in the epitaxial layer each having a second conductivity type opposite the first conductivity type. The first and second regions extend from a surface of the epitaxial layer opposite the substrate into the epitaxial layer to form respective first and second junctions therewith.

The first region defines a power section integrated in the epitaxial layer, and the second region defines a signal processing section integrated in the epitaxial layer. The power section and/or the signal processing section includes a

bipolar transistor and/or a DMOS transistor. First and second electrodes are also included for independently biasing the first and second junctions, respectfully.

Further, the integrated circuit also includes an isolating element positioned between the first and the second regions and extending from the surface of the epitaxial layer at least as far as a top surface of the substrate for reducing an injection of current through the epitaxial layer from the first region to the second region when the first junction is biased to cause the injection of current. The isolating element partially surrounds at least one of the first and second regions.

Furthermore, the isolating element also terminates above a bottom surface of the substrate. Independent Claims 12 and 22 are directed to related integrated circuits and have similarly been amended to recite that the first region defines a power section integrated in the epitaxial layer, and the second region defines a signal processing section integrated in the epitaxial layer. The power section and/or the signal processing section includes a bipolar transistor and/or a DMOS transistor. Further, the integrated circuit of Claims 12 and 22 also includes an isolating element positioned between the first and the second regions for reducing an injection of current through the epitaxial layer from the first region to the second region when the first junction is biased to cause the injection of current.

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II. The Claims are Patentable

Claims 12-26 were rejected in view of Hunter et al. (U.S. 4,631,803) in view of Yamaguchi et al. (IEEE) together or in various combinations with Nakagawa (U.S. 6,239,465) and/or Mavencamp (U.S. 6,175,277) for the reasons set forth on pages 3-11 of the Office Action. Applicant contends that Claims 12-26 clearly define over the cited references, and in view of the following remarks, favorable reconsideration of the rejections under 35 U.S.C. §103 is requested.

The Examiner has primarily relied on the Hunter et al. patent as disclosing an isolating trench for the purpose of "suppressing latch-up in CMOS devices." Furthermore, the Examiner combined the teachings of Hunter et al. with the CMOS deep-trench isolation structure of Yamaguchi et al. to allegedly meet the features of the present invention.

As noted above, each of the independent claims has been amended to recite a Bipolar-CMOS-DMOS (BCD) integrated circuit including first and second regions in the epitaxial layer each having a second conductivity type opposite the first conductivity type. The first region defines a power section integrated in the epitaxial layer, and the second region defines a signal processing section integrated in the epitaxial layer. The power section and/or the signal processing section includes a bipolar transistor and/or a DMOS transistor.

Additionally, each of the independent claims recites that the isolating element is positioned between the first and the second regions for reducing an injection of current

through the epitaxial layer from the first region to the second region when the first junction is biased to cause the injection of current. It is these combinations of features which are not fairly taught or suggested in the cited references and which patentably define over the cited references.

As emphasized by the Examiner, each of the cited references, and their corresponding teachings, is directed to and concerned with latch-up problems in CMOS devices. However, none of the cited references discloses a Bipolar-CMOS-DMOS (BCD) integrated circuit. None of the references discloses a first region defining a power section integrated in the epitaxial layer, and a second region defining a signal processing section integrated in the epitaxial layer, as claimed. Moreover, none of the cited references discloses a power section and/or signal processing section including a bipolar transistor and/or a DMOS transistor, as claimed.

Indeed, none of the cited references teaches the use of an isolating element positioned between the first and the second regions for reducing an injection of current through the epitaxial layer from the first region to the second region when the first junction is biased to cause the injection of current in a Bipolar-CMOS-DMOS integrated circuit having a power section, signal processing section, a bipolar transistor and/or a DMOS transistor, as claimed. In BCD structures, the signal processing section can be negatively affected by the injecting current generated by the power section. This has

been a longstanding problem which has not been satisfactorily solved.

There is simply no teaching or suggestion in the cited references to provide the combination of features as claimed. Accordingly, for at least the reasons given above, Applicant maintains that the cited references do not disclose or fairly suggest the invention as set forth in Claims 12, 17 and 22. Furthermore, no proper modification of the teachings of these references could result in the invention as claimed. Thus, the rejections under 35 U.S.C. §103(a) should be withdrawn.

It is submitted that the independent claims are patentable over the prior art. In view of the patentability of the independent claims, it is submitted that their dependent claims, which recite yet further distinguishing features are also patentable over the cited references for at least the reasons set forth above. Accordingly, these dependent claims require no further discussion herein.

Additionally, The Examiner objected to Claim 19 as being "a substantial duplicate of claim 13." Applicant respectfully traverses the Examiner's assertion because Claim 13 includes (via independent Claim 12) the "isolating element comprising a dielectric material adjacent said epitaxial layer and polycrystalline silicon spaced apart from said epitaxial layer by said dielectric material" (emphasis added) and only sets forth that the isolating element "partially surrounds said first region" which is not duplicative of any recitations

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in Claim 19. Accordingly, the Examiner's objection should be withdrawn.

III. Conclusion

In view of the foregoing remarks, it is respectfully submitted that the present application is in condition for allowance. An early notice thereof is earnestly solicited. If, after reviewing this Response, there are any remaining issues which need to be resolved before the application can be passed to issue, the Examiner is invited and respectfully requested to contact the undersigned by telephone to resolve such issues.

Respectfully submitted,

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CERTIFICATE OF FACSIMILE TRANSMISSION

I HEREBY CERTIFY that the foregoing correspondence has been forwarded via facsimile number 703-308-7722 to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 this 3rd day of October, 2003.

Dawn K. Kinder